RF Circuit Design In Reliability

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Abstract — **A methodology for designing reliable RF circuits is proposed. A model to predict hot carrier and soft breakdown effects on CMOS device parameters in RF circuits is developed. Hot carrier and soft breakdown effects are evaluated experimentally with 0.16 μm CMOS technology. Device stress measurement and SpectreRF simulation are conducted to evaluate the impact of hot carrier and soft breakdown effects on RF circuits such as low noise amplifier and voltage-controlled oscillator performance. Two design techniques to build reliable RF circuits are proposed and verified.**

I. INTRODUCTION

With the exploding development of wireless communications, it is desirable to integrate the whole transceiver on a single chip, and as CMOS technology advances, CMOS is becoming a promising candidate. However, with the transceiver blocks being integrated on the same chip, the circuit reliability is becoming more important than ever before. Reliability design should be an important part for any RF circuit. Hot carrier (HC) effect and soft breakdown (SBD) are two important issues for submicrometer CMOS devices and circuits. As CMOS device sizes shrink, the channel electric field becomes higher and HC effect becomes more significant [1] [2]. When the oxide is scaled down to less than 3 to 5 nm, SBD often takes place [3]. As a result, oxide trapping and interface generation cause long term performance drift and related reliability problems in devices, and in turn, the RF circuit performance will be also impacted by HC and SBD effects. Degradation of the DC device parameters has received widespread attention [1], but the degradation of RF circuit performance has not been studied systematically. The important reason is that no good methodology has been developed. The reported works usually apply the extracted stressed device models to every transistor in RF circuits, which makes the evaluation inaccurate.

In this paper, a systematical method to build reliable RF circuits is proposed, which combines device stress measurement and SpectraRF simulation. A model for predicting device parameter aging caused by HC and SBD effects in RF circuits is developed. The C_{gs} degradation is included in the aged model files for the first time, which makes the evaluation more accurate.

II. METHODOLOGY FOR RF CIRCUIT DESIGN IN RELIABILITY

The methodology to evaluate RF circuit reliability is shown in Fig. 1. The CMOS devices are stressed, and the aged device parameters are extracted. By simulating the specific RF circuit, the stress condition can be used to predict the device aging for the circuit using the proposed model. And then the aged model is used to predict the RF circuit performance degradations using SpectraRF simulation.

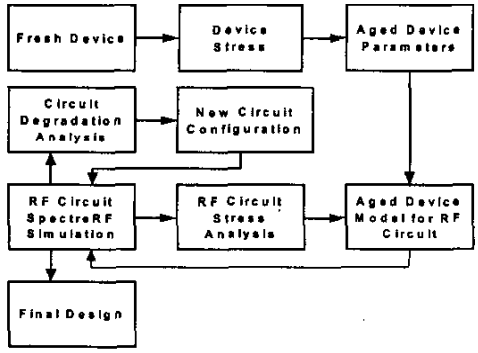

Fig. 1 Methodology for RF circuit design in reliability

The devices used in this work are 0.16 μm MOSFETs with the gate width of 10 μm and 50 μm, the gate oxide thickness of 2.4 nm, and the threshold voltage of 0.4 volt. The wafer is probed with the Cascade 12000 probe station and Agilent 4156B Precision Semiconductor Parameter Analyzer for stress measurements, while the RF experiments up to 50 GHz are carried out using Agilent 8510C Network Analyzer.

To mimic the circuit operation condition, the gate oxide stress and channel hot carrier effects are applied simultaneously. The source and body are grounded during stress. It is found that the breakdown voltage is about 3 volts. To enhance the hot electron degradation, the accelerated stress condition is set at $V_g = V_d = 2.6$ V. S-parameters of dummy pads on the same wafer are also measured and used for de-embedding the pad parasitic effects. The cutoff frequency of the device is extracted from the S-parameter measurements.

The measured device parameter degradations are shown in Fig. 2. After 3.5 hours stress, the threshold voltage and

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mobility degradations are about 40% and 45%, respectively; the transconductance and cut-off frequency degradations are about 27% and 43%, respectively.

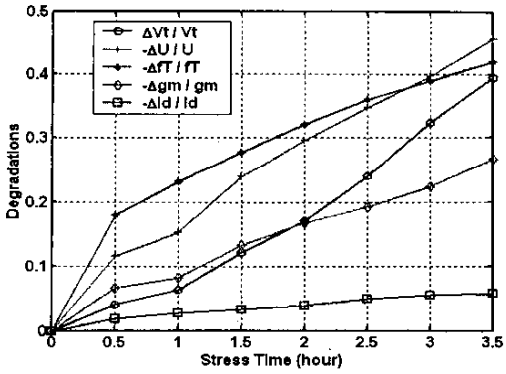

Fig.2 Measured device parameter degradations

Due to the threshold voltage and the mobility degradations, the drain current is also degraded about 5.8%.

In the past works, only threshold voltage and mobility degradations are included in the aged model file when evaluating the RF circuit performance degradations. Device capacitances degradations are not included. In reality, capacitances can also impact RF performance significantly and cannot be ignored. The measured gate capacitance degradation is shown in Fig. 3.

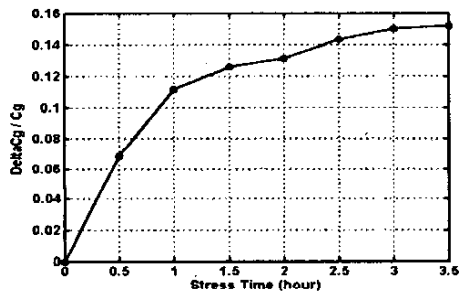

Fig. 3 C_g degradation

To predict the device parameter degradations in a specific RF circuit, a model is needed to build the relationship between the experimental data and the aged file for the circuit. The HC induced device degradations are correlated to the substrate current and the gate current for n-MOSFETs and p-MOSFETs, respectively. For n-MOSFETs, the correlation exists because hot carriers and substrate current I_{sub} are driven by the maximum channel electric field, which occurs at the drain end of the channel. For p-MOSFETs, the charge trapping in the gate oxide is the dominant driving force for degradation, so the degradation is correlated with the gate current.

To evaluate the degradations of devices, the substrate current model is created in (1) as a function of V_{gs} and V_{ds} [4]:

$$I_{sub}(V_{gs},V_{ds}) = \frac{A_i}{B_i}(V_{ds}-V_{dsat}(V_{gs}))I_{ds}(V_{gs})e^{\frac{-B_i \cdot l_c}{V_{ds}-V_{dsat}(V_{gs})}} \quad (1)$$

where $l_c = (l_{c0} + l_{c1}V_{ds})\sqrt{t_{ox}}$ is a bias dependent factor, A_i, B_i, l_{c0} and l_{c1} are the technology dependent factors, $V_{dsat} = \frac{E_{crit0}L_{eff}(V_{gs}-V_t)}{E_{crit0}L_{eff}+V_{gs}-V_t}$, E_{crit0} is the critical electric field, and L_{eff} is the effective channel length.

In the evaluation of device lifetime, the degradation of parameter is given by [4]

$$\Delta D = \left(\frac{I_{ds}}{HW}\left(\frac{I_{sub}}{I_{ds}}\right)^m t\right)^n \quad (2)$$

where H, m and n are technology dependent factors, t is the stress time, and W is the channel width.

These models are applied to devices, and the degradations due to HC and SBD effects are evaluated by experiments and simulations.

After H, m, and n are extracted, they are used to predict the degradations of device parameters. For the threshold voltage, $n = 0.43907$, $m = 1.37539$, and $H = 1.37673\times10^6$. The calculated threshold voltage degradation is shown in Fig. 4, where V_{gs} and V_{ds} are 0.75 volt and 1 volt, respectively.

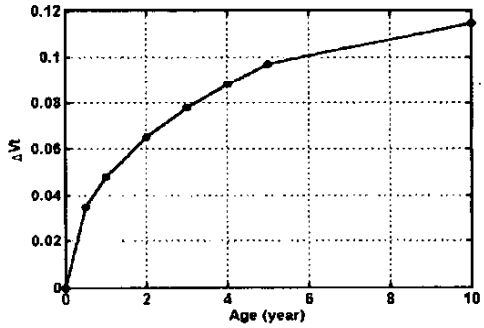

Fig. 4 Calculated threshold voltage shift as a function of time

Same methodology can be applied to other device parameters such as mobility and C_g, and the aged device parameters can be used to evaluate the RF circuit performance degradations.

III. RF CIRCUIT DEGRADATIONS

It is clear from Section II that CMOS devices are degraded significantly subject to HC and SBD effects. It is expected that CMOS RF circuit performance will also be degraded. Performance degradation in an LNA and a VCO due to HC and SBD effects are evaluated in this section using the proposed methodology.

Since the LNA is the first important block in receiver, it determines, to a large extent, the sensitivity of the receiver. However it is very sensitive to noises and interferences. A low noise amplifier that works at 5 GHz in Wireless LAN communication systems is displayed in Fig. 5. The figures of merit of LNA include gain, impedance matching, noise figure and linearity properties.

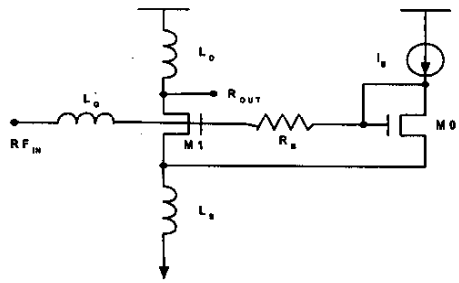

Fig. 5 A low noise amplifier for Wireless LAN application

To evaluate HC and SBD effects on this LNA circuit's performance, the 0.16 μm technology NMOS device was stressed and the degraded device parameters were extracted. Using the proposed methodology, the LNA S-parameter degradations with respect to operation time are shown in Fig. 6. It is shown that S11 and S21 change significantly within the first year. S11 degrades about 9 dB at 5 GHz. This is because of significant changes in the equivalent input components of the transistor such as C_{gs} and g_m that tend to degrade the input impedance matching dramatically. The gain degradation is about 0.55 dB, mainly due to the decrease of the transconductance of the transistor.

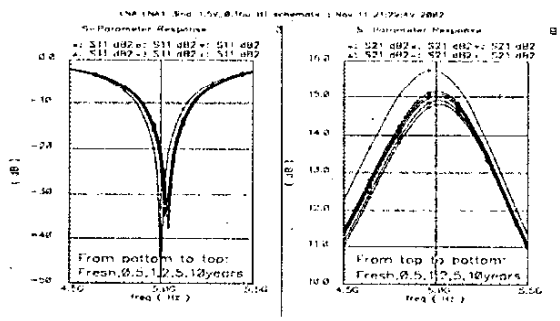

Fig. 6 Simulated S-parameters versus frequency

The normalized noise figure taking into account of ΔC_{gs}, ΔV_T, and $\Delta\mu$ is given as

$$\frac{\Delta F}{F}=\frac{1+\frac{\Delta C_{gs}}{C_{gs}}+\left(1+\frac{\Delta\mu}{\mu}\right)\left(1-\frac{\Delta V_T}{V_{gs}-V_T}\right)}{\frac{K\cdot\alpha\cdot G_S(\mu+\Delta\mu)(V_{gs}-V_T-\Delta V_T)(L_G+L_S)}{\gamma\cdot C_{gs}}+\left(1+\frac{\Delta\mu}{\mu}\right)\left(1-\frac{\Delta V_T}{V_{gs}-V_T}\right)} \quad (3)$$

where K, G_s, α and γ are all constants.

This equation gives a guideline for designing a LNA with lower noise figure.

The most important parameter for VCO is phase noise. In order to predict the degradation of VCO phase noiser due to HC and SBD effects, a 5-stage ring VCO composed of 5 fully differential delay stages is examined. As shown in Fig. 7, each delay cell consists of NMOS differential pairs with PMOS resistive loads. The gate voltage V_g is controlled carefully by a replica biasing circuit (not shown here) so that the PMOS transistors are working in the linear region and the voltage swing is kept constant.

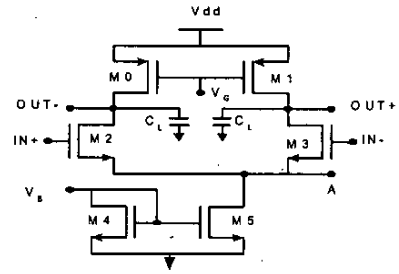

Fig. 7 Schematic of delay cell in VCO

To evaluate the performance degradation of a VCO due to HC and SBD effects, the proposed methodology is used. The simulated VCO phase noise degradation is displayed in Fig. 8 (Original). It is clear from Figs. 8 that the VCO performance is degraded significantly in the first 2 years. The phase noise degradation is about 3 dB.

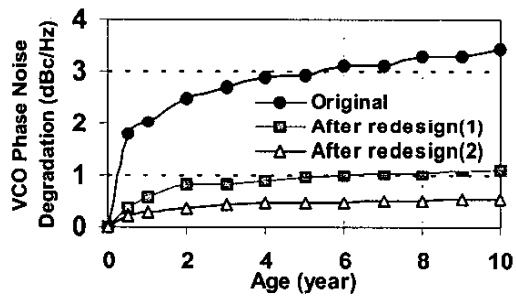

Fig. 8 VCO phase noise degradation versus age

IV. Design Techniques To Reduce HC and SBD Effects On RF Circuits

In order to reduce the HC and SBD effects on RF circuits, two techniques are proposed in this section. The first technique is to use a cascode structure. HC effect is caused by high voltage drop between the drain and source of the transistors in the circuits. If V_{ds} is reduced, the HC effect is expected to reduce. The Cascode structure can achieve this goal. SBD effect can be reduced by decreasing the voltage swings. An improved LNA circuit is demonstrated in Fig. 9. The S-parameter degradations of the improved LNA are shown in Fig. 10.

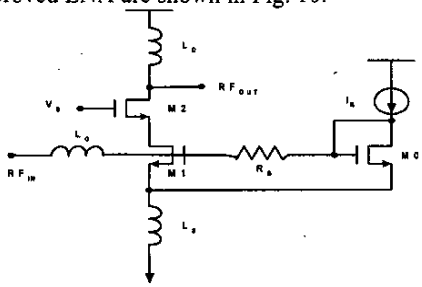

Fig. 9 An improved LNA design

It is shown that the improved LNA is not sensitive to HC and SBD effects.

The normalized noise figure can be calculated using (4):

$$\frac{\Delta F}{F}=\frac{1+\dfrac{\gamma\cdot\Delta C_{gs}}{\gamma\cdot C_{gs}+G_s^2\delta\cdot\zeta(L_g+L_s)}-\left(1+\dfrac{\Delta\mu}{\mu}\right)\left(1-\dfrac{\Delta V_T}{V_{gs}-V_T}\right)}{\dfrac{KG_s(\mu+\Delta\mu)(V_{gs}-V_T-\Delta V_T)(L_G+L_S)}{\gamma\cdot C_{gs}+G_s^2\delta\cdot\zeta(L_G+L_S)}+\left(1+\dfrac{\Delta\mu}{\mu}\right)\left(1-\dfrac{\Delta V_T}{V_{gs}-V_T}\right)} \quad (4)$$

where K, G_s, γ, δ and ζ are all constants.

The cascode structure can also be applied to the VCO circuit in Fig. 11. The phase noise simulation result is shown in Fig. 8 (after redesign (2)). And the s-parameter simulation result is shown in Fig. 10. The new circuit has much lower phase noise, and much more reliable.

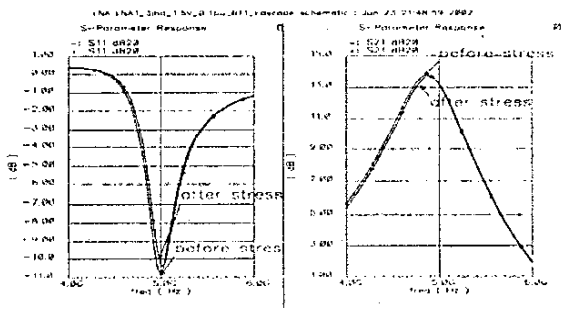

Fig. 10 Simulated S-parameter versus frequency

Another design technique to reduce HC and SBD effects is to adjust the parameters of the RF circuit and make it less sensitive to device parameter shifts. In the VCO delay cell in Fig. 7, the channel width of the differential pair was 2 μm. After stress the circuit simply cannot work because of the device parameter shifts. This means that the circuit is very sensitive to HC and SBD effects. To reduce HC and SBD effects, the channel width of differential pair is changed from 2 to 5 μm to provide a larger current. The phase noise degradations are then demonstrated in Fig. 8 (After redesign (1)). It is shown that the phase noise degradation with Wm3 = 5 μm is only about 1.1 dB. The improvement of phase noise is significant with larger power dissipation.

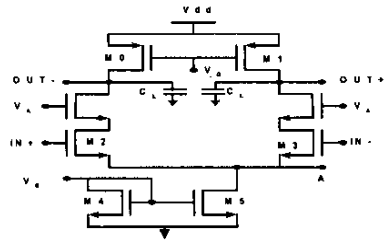

Fig. 11 Improved VCO delay cell

V. Summary

A methodology to design RF circuit in reliability is proposed. Hot carrier and soft breakdown effects on RF circuit performance are examined. A model to predict the aging of the device parameters in RF circuits is developed. The methodology uses the aged model files from accelerated stress and combines with SpectreRF simulation to evaluate RF circuit performance degradation. Examples of low noise amplifier and voltage-controlled oscillator as a function of stress age are shown. Two redesign techniques are proposed. The use of cascaded structure significantly reduces hot carrier degradation and therefore enhances the circuit performance against aging.

References

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